IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)

    FARMWALD ET AL.   )

Serial No: **09/252,997**   )   U.S. Patent No. : **6,034,918**

Filed: February 19, 1999   )

Title: METHOD OF OPERATING A MEMORY   )
           HAVING A VARIABLE DATA OUTPUT   )
           AND A PROGRAMMABLE REGISTER   )

Commissioner of Patents and Trademarks
Washington, D.C. 20231

TRANSMITTAL LETTER

Dear Sir:

    With respect to the above-identified patent, transmitted herewith is a **REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR § 1.322**. No fee is required. However, should a fee be required, it is to be paid as indicated below:

[   ]   A check payable to the Commissioner of Patents and Trademarks, in the amount of $\underline{\$\hspace{2cm}}$ is enclosed as payment of the Total Fee Due.

[   ]   Please charge our Deposit Account No. <u>50-0998</u> in the amount of $\underline{\$\hspace{1.5cm}}$ to cover the above fees. A duplicate copy of this sheet is enclosed.

[**XX**]   The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. <u>50-0998</u>. A duplicate copy of this sheet is enclosed.

                                 Respectfully submitted,

Date: June 14, 2000   By: _____

                                   Neil A. Steinberg
                                   Registration No. 34,735
                                   650-944-7772

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Application of:

FARMWALD, ET AL.

Serial No.: 09/252,997

Patent No. **6,034,918**

Filed: FEBRUARY 19, 1999

Title: METHOD OF OPERATING A
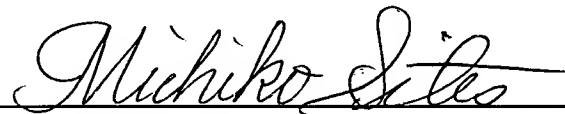MEMORY HAVING A VARIABLE DATA
OUTPUT AND A PROGRAMMABLE
REGISTER

Assistant Commissioner for Patents
Washington, DC 20231

Certificate of Mailing Under 37 CFR 1.8

I hereby certify that the attached **1)** Transmittal Letter (1 page and 1 copy

thereof), **2)** Request for Certificate of Correction (3 page and 2 exhibits attached) and

3) Certificate of Correction (1 page) is/are being deposited with the United States Postal

Service with sufficient postage as first class U.S. mail in an envelope addressed to:

Assistant Commissioner for Patents
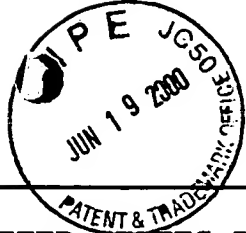Washington, D.C. 20231

On June 15, 2000.

_____
(Signature)

Michiko Sites

_____
(Print Name of Person Signing Certificate)

In the Application of:)

)

       FARMWALD ET AL.   )

)

Serial No.: **09/252,997**   ) Patent No.: **6,034,918**

)

Filed: **February 19, 1999**   )

)

Title: **METHOD OF OPERATING A MEMORY**)
       HAVING A VARIABLE DATA OUTPUT)
       LENGTH AND A PROGRAMMABLE)
       REGISTER)

Commissioner of Patents and Trademarks
Washington, DC 20231

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR § 1.322

Dear Sir:

    It is respectfully requested that the Commissioner issue the attached Certificate of Correction to correct typographical errors in U.S. Patent 6,034,918 ("the '918 patent", copy attached as Exhibit 1). In particular, the attached Certificate of Correction seeks to correct errors in claims 13-16 and claims 35-38. Claims 13-16 should have been printed as being dependent on claim 1 rather than being dependent on claim 11, as they were printed in the '918 patent. Claims 35-38 should have been printed as being dependent on claim 34 rather than being dependent on claim 32, as they were printed in the '918 patent

    The Preliminary Amendment of February 19, 1999, copy attached as Exhibit 2, clearly discloses claims 163-166 being dependent on

APPROVED

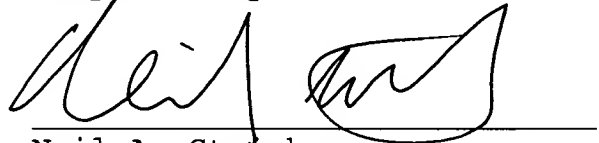DEC 0 7 2000

FOR THE DIRECTOR OF USPTO

claim 151. Claim 151 was renumbered claim 1 in the '918 patent and claims 163-166 were later renumbered claims 13-16, respectively. There were no subsequent amendments of the above-referenced application which affected the claim dependency of claims 163-166 (i.e., claims 13-16 in the '918 patent).

In addition, the Preliminary Amendment of February 19, 1999 clearly discloses claims 185-188 being dependent on claim 184. Claim 184 was renumbered claim 34 in the '918 patent and claims 185-188 were later renumbered claims 35-38, respectively. There were no subsequent amendments of the above-referenced application which affected the claim dependency of claims 185-188 (i.e., claims 35-38 in the '918 patent).

This error incurred through the fault of the U.S. Patent and Trademark Office ("USPTO"), as is clearly disclosed by the records in the USPTO.

It is respectfully requested that the attached Certificate of Correction issue. It is noted that should a telephone interview expedite consideration of this request in any way kindly contact Neil Steinberg at 650-944-7772.

Respectfully submitted,

Date: June 14, 2000

Neil A. Steinberg
Attorney of Record
Reg. No. 34,735
650-944-7772

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 6,034,918

DATED   : Mar. 7, 2000

INVENTOR(S): Farmwald et al.

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In Col. 25, on line 62, delete "11" and substitute --1--.

In Col. 25, on line 65, delete "11" and substitute --1--.

In Col. 26, on line 1, delete "11" and substitute --1--.

In Col. 26, on line 6, delete "11" and substitute --1--.

In Col. 28, on line 16, delete "32" and substitute --34--.

In Col. 28, on line 18, delete "32" and substitute --34--.

In Col. 28, on line 21, delete "32" and substitute --34--.

In Col. 28, on line 33, delete "32" and substitute --34--.

MAILING ADDRESS OF SENDER:

Neil A. Steinberg
Rambus Inc.
2465 Latham Street
Mountain View, CA 94040

PATENT NO. 6,034,918

No. of additional copies

⇨

United States Patent [19]

Farmwald et al.

[54] **METHOD OF OPERATING A MEMORY HAVING A VARIABLE DATA OUTPUT LENGTH AND A PROGRAMMABLE REGISTER**

[75] Inventors: **Michael Farmwald**, Berkeley; **Mark Horowitz**, Palo Alto, both of Calif.

[73] Assignee: **Rambus Inc.**, Mountain View, Calif.

[56] References Cited

U.S. PATENT DOCUMENTS

3,821,715 6/1974 Hoff, Jr. et al. 340/172.5
4,092,665 5/1978 Saran 341/63

(List continued on next page.)

OTHER PUBLICATIONS

T.L. Jeremiah et. al., "Synchronous Packet Switching Memory and I/O Channel," IBM Tech. Disc. Bul,. vol. 24, No. 10, pp. 4986–4987 (Mar. 1982).

L. R. Metzeger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562–567 (Oct. 1983).

A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two–Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57–61 (Feb. 1989).

D.T. Wong et. et al., "An 11–ns 8Kx18 CMOS Static RAM with 0.5–μm Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095–1103 (Oct. 1988).

T. Williams et. al., "An Experimental 1–Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085–1094 (Oct. 1988).

D. Jones, "Synchronous static ram", Electronic and Wireless World, vol. 93, No. 1622, pp. 1243–1244 (Dec. 1987).

F. Miller et. al., "High Frequency System Operation Using Synchronous SRAMS", Midcon/87 Conference Record, pp. 430–432 Chicago, Il., USA; Sep. 15–17, 1987.
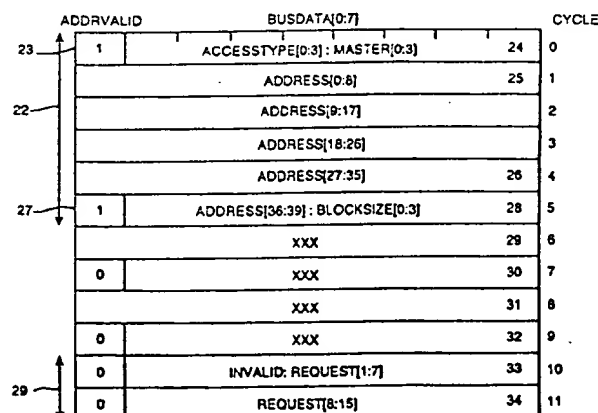
(List continued on next page.)

[57] ABSTRACT

A method of controlling a memory device is disclosed wherein the memory device includes a plurality of memory cells. The method comprises providing first block size information to the memory device, wherein the first block size information defines a first amount of data to be output onto a bus in response to a read request. The method further includes issuing a first read request to the memory device, wherein in response to the first read request, the memory device outputs the first amount of data corresponding to the first block size information onto the bus synchronously with respect to an external clock signal. In one preferred embodiment, the method may include providing a code which is representative of a number of clock cycles of the first and second external clock which are to transpire before data is output by the memory device onto the bus. The memory device stores the code in a programmable register on the memory device. In this preferred embodiment, the first amount of data corresponding to the first block size information is output after the number of clock cycles of the external clock transpire.

38 Claims, 15 Drawing Sheets

ADDRVALID	BUSDATA[0:7]		CYCLE
1	ACCESSTYPE[0:3] : MASTER[0:3]	24	0
	ADDRESS[0:8]	25	1
	ADDRESS[9:17]		2
	ADDRESS[18:26]		3
	ADDRESS[27:35]	26	4
1	ADDRESS[36:39] : BLOCKSIZE[0:3]	28	5
	XXX	29	6
0	XXX	30	7
	XXX	31	8
0	XXX	32	9
0	INVALID: REQUEST[1:7]	33	10
0	REQUEST[8:15]	34	11

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FARMWALD ET AL.)
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Serial No: **09/252,997**) U.S. Patent No. : **6,034,918**
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HAVING A VARIABLE DATA OUTPUT)
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Commissioner of Patents and Trademarks
Washington, D.C. 20231
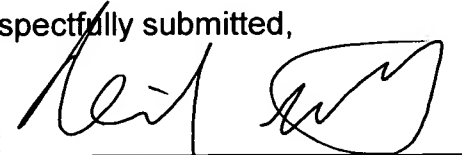
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650-944-7772